SiGe MEMS technology

Introduction

Micro-electromechanical systems (MEMS) devices require an integrated circuit for signal conditioning. Combining MEMS and its electronics can be done either by using a hybrid approach, in which CMOS and MEMS are developed on separate chips that are assembled together afterwards, or by using a monolithic approach, in which co-integration by using a special process flow allows for a single chip/single package solution. About half of the current MEMS market uses a hybrid approach and half a monolithic approach.

Hybrid integration has the advantage of a fast time to market and allows for an independent optimization of the integrated circuit (IC) and the MEMS technology. On the other hand, the assembly and packaging cost is higher in comparison to the monolithic approach. This is certainly the case if a large number of interconnections need to be made or for small chips. Consequently, the longer development time needed for the monolithic approach can be paid back by the reduced assembly and packaging cost for chips having a size below a critical area, which depends on the complexity of the MEMS process, for chips having more interconnections than a certain critical number and for large volumes. Monolithic integration can also be chosen in cases where an increase in system performance is required. When separate chips for the MEMS and the IC are used, performance-limiting parasitics are present due to the interconnections between the MEMS and logic chip. These parasitics result mainly from the size of the bond pads and from the long bonding wires and are reduced substantially by on-chip integration.

IMEC proposes a monolithic approach for MEMS on top of CMOS using SiGe as structural material. Contrary to the other types of monolithic approaches, as MEMS first or MEMS interleaved in the CMOS process, the IMEC approach provides a high degree of modularity, like use of low cost and state of the art CMOS foundries. Furthermore, it is best suited for high volume and reduced area size products requiring low power consumption and high performance. Several

functionalities can be combined on the same chip (eg. multi-axes accelerometers and gyroscopes) giving an additional degree of freedom for designers to reduce the complexity of the CMOS signal conditioning. Monolithic approach is often also the only available solution for dense array applications such as imagers or scanning probe systems for memory applications.

CMORE program and the SiGe MEMS platform

IMEC has set up a 'CMORE' research and development platform for customized, Si-based processing technologies, to offer cost-effective solutions for monolithic co-integration of heterogeneous technologies. The platform focuses on IC manufacturing processes and devices that incorporate new functions and optimize specific performance, rather than relying on continued scaling of the transistor dimensions. The CMORE services offered range from development-on-demand, over prototyping, to low-volume production. These services profit from the expertise in many research areas available at IMEC. The CMORE solutions are implemented in IMEC's 200mm fab with advanced packaging capabilities. There are two process platforms involved: a 0.13µm CMOS process and a versatile SiGe above-IC MEMS process which can be used separately or combined.

The IMEC MEMS-PLATFORM technology (MEMS PT) is designed for the monolithic integration of CMOS and MEMS. It is built to address a large number of applications by providing a baseline process consisting of a CMOS protection module, the electrical connection to the CMOS metallization, the electrode module with thin and thick electrode, the sacrificial layer deposition and etch module, the structural layer module with also 2 different thicknesses and a bondpad/packaging module. The structural layer can be tuned towards the demonstrator specifications and a choice of functional modules (optical, electrical, probes, piezoresistive sensors) can be added for specific demonstrator functionality. The SiGe structural layer guarantees the desired material properties and its low deposition temperature (450ºC) retains the performance and reliability of the CMOS electronics. The baseline process is depicted in figure 1.

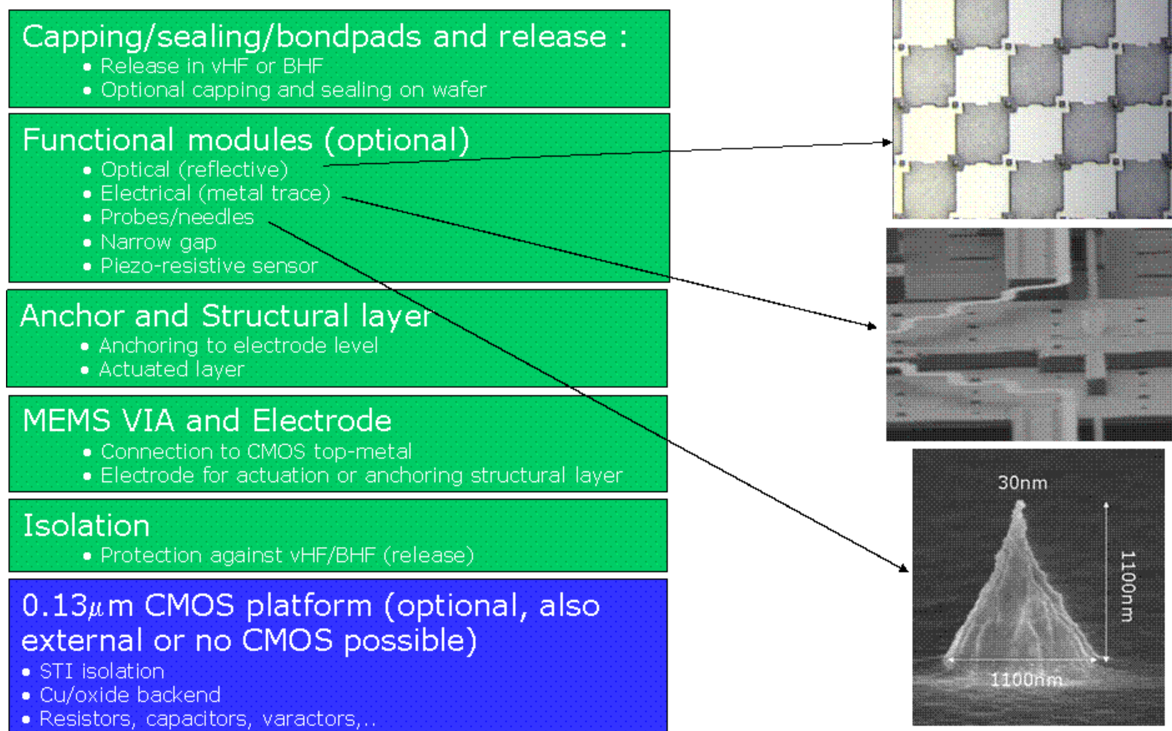

Figure 1: Schematic process flow.

The MEMS devices are connected to the top CMOS metal layer through SiGe or W plugs. A thick SiC layer protects the CMOS during the vapor HF release process. After electrode patterning, oxide deposition and chemical-mechanical polishing (CMP) ensure a flat wafer surface. Thus, a well-controlled gap can be achieved by the sacrificial layer deposition process. The structural layer module consists of an anchor patterning followed by a SiGe deposition and patterning. A few hundred of nanometers of conformal chemical-vapor deposition (CVD) SiGe is deposited to ensure good structural layer crystallization and anchor filling. Afterwards, the remainder of the structural layer is formed by plasma-enhanced chemical-vapor deposition (PECVD) deposition, with a much faster deposition rate compared to CVD process. The deposition of the CVD/PECVD SiGe structural layer is optimized to minimize the deposition time (cost, cycle time) and the strain gradient (as low as 10^{-6}/µm).

At this point, specific functional modules, such as a reflective Al layer for optical devices, Pt metal lines for electrical connections or sharp tips can be added on top

of the structural layer. Some of these functional modules require trenches to be filled with oxide and planarised by CMP after structural layer patterning.

An optional SiGe thin-film capping module (under development) to protect the MEMS devices can be added next. Release holes perforate the SiGe device and cap membrane and the oxide sacrificial layer is removed during vapor HF release. In case thin-film packaging is chosen, a sealing module will hermetically seal the package. Bond pads are then formed at the end of the process to allow CMOS/MEMS probing.

The MEMS-PT modularity delivers the necessary flexibility to satisfy the different application needs. A specific module at the electrode and structural layer levels allows single or dual thickness processes. Two different thicknesses for the electrode module can provide more flexibility to the designer to tune the actuation voltage and to have a better control over the mechanical movement. At structural layer level, thinner springs can reduce the spring constant, the actuation voltage and therefore the power consumption. As the major part of the structural layer can keep its original thickness, the required structural layer flatness and mechanical properties are preserved, see figure 3. The dual thickness option is, both for electrode and structural layer level, realized by adding a hard mask (HM). The electrode or structural layer deposition is broken into two steps to embed a 250nm oxide HM that protects the underlying SiGe layer during SiGe etch.

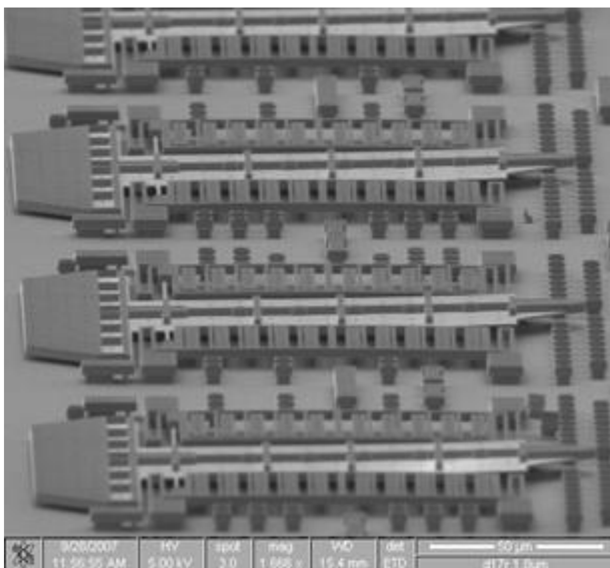

Figure 2: Flat cantilevers made with a combination of thin and thick SiGe structural layers [1].

All modules have been evaluated for process control and yield. In figure 4 a cross-section SEM (XSEM) image of the SiGe plug/SiGe electrode layer for the electrode module is shown. Contact resistance values have been reduced down to 40 Ohm for a 0.8µmx0.8µm square contact by using special cleaning techniques and extra adhesion layers. An alternative W electrode module has also been developed for RF applications leading to a contact resistance as low as 10Ohm for a 0.6µmx0.6µm square contact size.

To ensure a high within-wafer and wafer-to-wafer uniformity and a high process yield, state-of-the art equipment for the SiGe deposits and for deep reactive ion etching of SiGe is used for this platform.

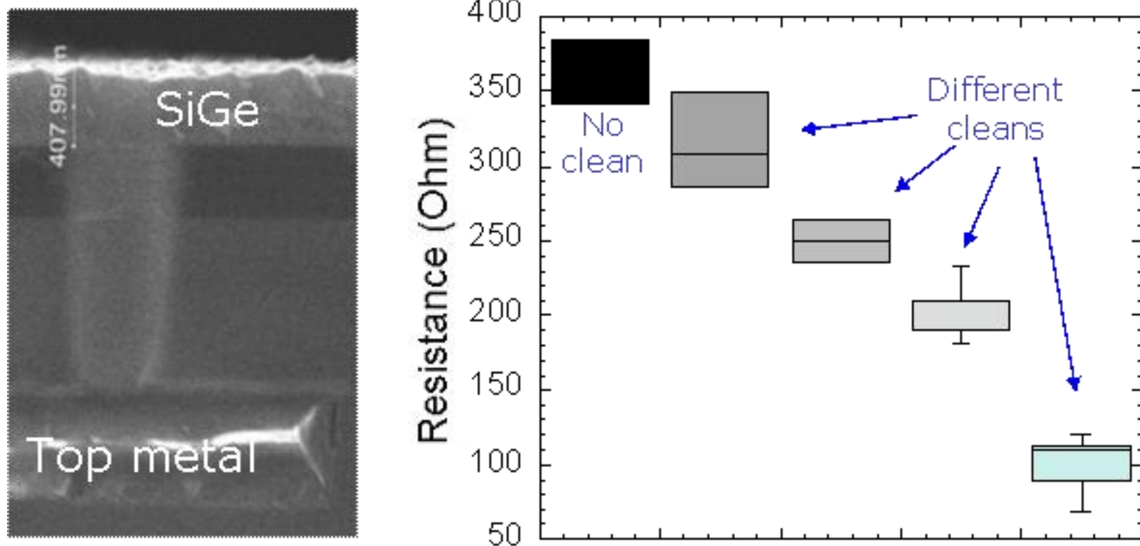

Figure 3: a) XSEM image of MEMS-via SiGe contact to Al last CMOS metal layer. b) MEMS-via resistance values (within wafer variation for 0.8µm x 0.8µm square contacts) for various contact interface clean processes before SiGe deposition [1].

CMORE applications

Poly-SiGe demonstrator: reliable 11 megapixel micro-mirror array for high end industrial applications

With the poly-SiGe MEMS platform described above, very reliable CMOS-integrated 10cm² 11 MPixel SiGe-based micro-mirror arrays were fabricated for the first time [2]. The array, which is to be used as spatial light modulator (e.g. for video projection, mask writers, optical maskless lithography) consists of 8µm x 8µm pitch pixels which can be individually addressed by an analog voltage to enable accurate tilt angle modulation. The pixel density is almost double compared to the state-of-the-art. Stable average cupping below 7nm, root mean square (RMS) roughness below 1nm and long lifetime (>10^{12} cycles, no creep) are demonstrated.

The 8µm pitch mirrors were processed on top of standard 0.18µm analog-CMOS wafers, fabricated by NXP, featuring 6 interconnect levels. A schematic view of the used process flow is shown in figure 4, while a photograph of the completed die is shown in figure 5. Poly-SiGe was chosen as structural material for the mirrors, instead of the commonly-used Al, as it solves many of the reliability issues of Al-based mirrors, and it is compatible with above CMOS processing, allowing a smooth integration with the CMOS chip below.

CMOS base wafer
Top level metal planarisation + passivation
SiC protection layer
W-vias
SiGe electrode + planarisation
Sacrificial oxide deposition
Mirror hinge formation
Sige mirror layer deposition + CMP
Phasestep etch (optional)
Mirror etch
Oxide protection + bondpads
Release

Figure 4: Schematic process flow of the micromirror module.

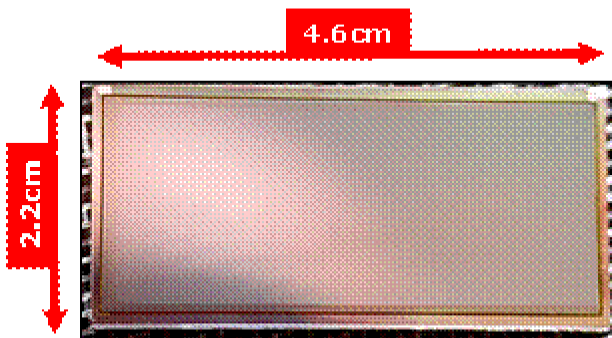

Figure 5: Photograph of the 10cm² die after release.

Cantilever array for scanning probe storage

Another project used the poly-SiGe MEMS platform to fabricate a cantilever array carrying a read/write tip for a scanning probe storage memory [1]. The cantilever is made in the structural layer and can be tilted using an underlying electrode around a torsional hinge, and move in plane driven by comb drives. In this cantilever array,

the dual thickness of the structural layer was used to be able to tune the stiffness of the cantilever and the stiffness of the torsional hinges independently. The tip is formed on top of the cantilever and connected using an additional suspended metal trace, see figure 3.

The future

For the automotive market it is predicted that the number of MEMS devices/vehicle will increase from 40 now to 60 in 2011. In order not to increase the size or the price of the cars, it is expected that more integration and a lower cost/device will be needed. Also, a stronger increase of the integrated MEMS market compared to the overall increase in MEMS market is predicted in market studies. The need for increased functionality/unit area and lower cost/device is translated into a first roadmap for MEMS integration (see figure 6). In this first roadmap [3] a lower cost/device is achieved by decreasing the area/ integrated device. Putting devices in an array clearly decreases the area/device as addressing of the individual devices is enabled by the CMOS below and common bondpads can be used. The integrated micro-mirrors shown above are a clear example of such an array. Thin-film packaging further decreases the area/device and thus also the cost. Our SiGe MEMS platform will in the near future enable the fabrication of thin film SiGe caps above CMOS-integrated MEMS devices, forming an area-saving MEMS-device-scale 0-level package. Ultimately this process enables the creation of highly integrated miniature systems with multiple packaged sensors and actuators post-processed on a single chip. This is also shown as the final stage in the envisioned SiGe roadmap using poly-SiGe processes at 400-450ºC. Extensions to this roadmap could come by the addition of other materials such as metals (e.g. for coils) or polymers (e.g. for temporary packaging, for low stiffness requirements…).
The need for more integration leads also to a need for more possibilities to integrate or more flexibility towards integration. This is possible by decreasing the processing temperature of the MEMS even further, allowing integration with other substrates such as integrated passives substrates or even polymer substrates. This is shown in the second roadmap [3], indicating the road towards ‘flexible’

MEMS integration (see figure 7). Crystallization tricks such as metal-induced crystallization or laser annealing can be used. Ultimately self-assembly techniques might be used to integrate MEMS on any type of substrate. Different driving forces (capillary, magnetic, dielectrophoresis…) can be used to self-assemble chips or individual devices on a substrate with electrodes. IMEC started a research project on the self-assembly of carbon nanotube (CNT)-based NEMS.

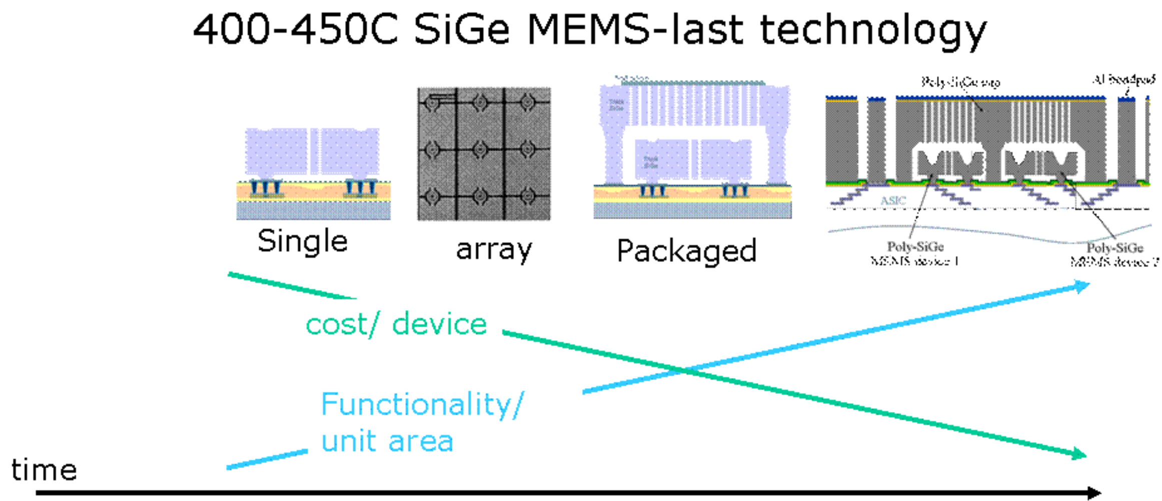

Figure 6: Envisioned roadmap for MEMS post-processing based on poly-SiGe deposited at 400 – 450ºC [3].

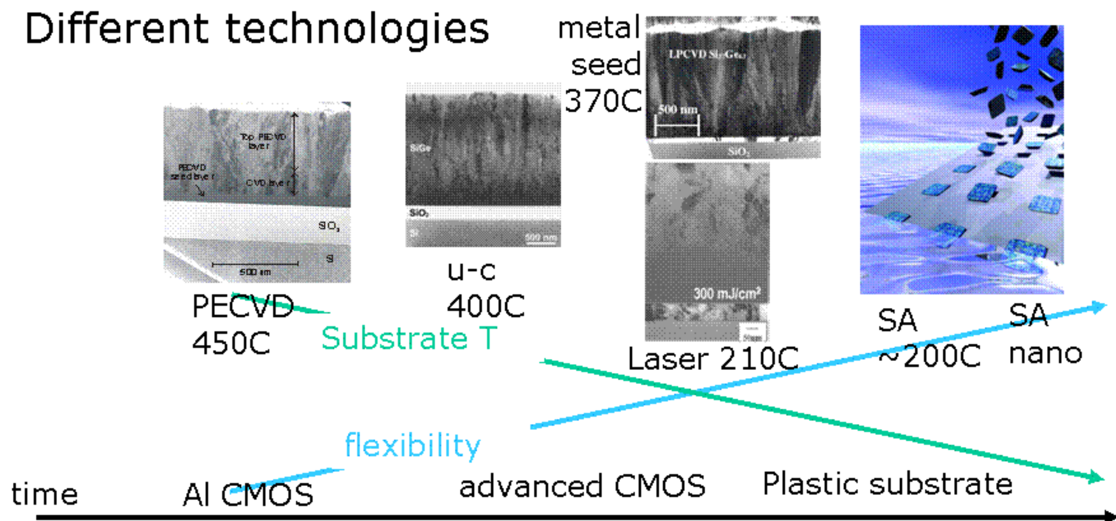

Figure 7: Envisioned roadmap for low temperature MEMS integration [3].

References

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Bio

Ann Witvrouw received an MS degree in Metallurgical Engineering in 1986 from the Katholieke Universiteit Leuven, Belgium, and both an MS degree in Applied Physics in 1987 and a Ph.D. degree in Applied Physics in 1992 from Harvard University, USA. Since 1992 she joined IMEC, Belgium where she worked on the reliability of metal interconnects until the end of 1998. During this time her research was focused on the mechanical stress in films and lines, electro-migration and stress induced voiding. In 1998 she switched to research in Micro-electromechanical Systems (MEMS) at IMEC, focusing on advanced MEMS process technologies. From 2000-2007 she was leading a team on MEMS integration, first as team leader and later as program manager. Currently she is a principal scientist in the MEMS/NEMS area. She has been the coordinator of the European IST projects SUMICAP and SiGeM and several industrial projects in the

area of MEMS integration. Currently she is coordinator of the Flemish SBO project Gemini.