
2008 INDUSTRY REPORT

FOCUS ON MEMS PACKAGING

EXECUTIVE SUMMARY

Members of the MEMS Industry Group (MIG) met in May 2008 at MIG's annual members' meeting - MEMS Technology Roadmap and Industry Congress (METRIC). Members convened to focus on critical issues affecting MEMS packaging; a very timely issue given the recent increase in the adoption and adaptation of MEMS. Attendees were divided into five working groups, determined by the METRIC 2008 steering committee, based on areas within MEMS packaging still facing commercialization issues. The goal of METRIC 2008 was to identify critical packaging issues and list potential deliverables, in order to benefit not only MIG members but the industry as a whole.

METRIC 2008 WORKING GROUPS

PACKAGING: A BACKEND OPERATION

This working group's objective was to determine strategic sequencing for MEMS packaging by establishing a three-step process—when to singulate, when to package, and when to test. In an effort to compile a series of best practice, the group focused on creating a MEMS device from the backend (i.e. from wafer to assembly).

The primary consensus of the group was that backend packaging should not be an afterthought. Several steps need to be considered: singulation, packaging, sacrificial layer removal, and testing. However, the group could not determine one superior process flow order; there are pros and cons to each approach. For discussion purposes, the group chose to look at Wafer-Level Packaging (WLP) to determine the advantages and disadvantages of that packaging process and actually determined that it's a four (not three) step process to package.

No surprise, cost was found to be a significant factor in determining process flow development stages. Furthermore, establishing a standard test is highly unlikely as all MEMS devices and fabs are rarely setup for such a process. Where to test and what to test are also obstacles and even the definition of testing (what constitutes a test?) was also debated.

What's needed, then, is a resource guide. This resource guide will be part of the MIG web site and will incorporate (non-proprietary) input from MIG members, on packaging terminology and success stories, working with foundries, and other related white papers.

UNIQUE PACKAGING STYLES—MEMS, CMOS, AND MULTICHIP INTEGRATION

The Unique Packaging Styles group discussed the growing trend toward integrating MEMS with CMOS, as well as MIG's role in advancing this integration. The group began by reviewing the critical factors in MEMS packaging that affect device performance; stress management topped this list. The conversation then moved to functional cap performers and the advent of Through-Silicon Vias (TSV). It was pointed out that new players entering the industry are primarily developing co-integrated devices, and additional testing requirements may need to be established for these devices.

As described earlier, METRIC attendees believed that packaging is often seen as an afterthought, resulting in a more expensive option. Multi-chip integration (enabling the use of existing infrastructures) was generally viewed as a significant way to reduce cost. Due to the recent rise in the price of gold, smart capping was mentioned as a more cost-effective solution. However, high volumes won't be achieved for at least another two years.

Most attendees admitted to preferring package-level integration over die-level integration. WLP is an interesting trend, though the current belief is that WLP is really more of a luxury for large companies with high volumes.

The group's major recommendation was for MIG to take a more active role in advancing packaging. This could be accomplished in several ways: educating the venture capital industry on the high cost of MEMS packaging; soliciting more packaging houses to become MIG members; publishing links on MIG's website for potential partners to help with small volume productions (a matchmaking service); as well as identifying general trends, common and newly developed processes, and creating a MEMS-wiki site.

WAFER-LEVEL AND 3-D INTEGRATION

What are the benefits and challenges of packaging at the wafer level? Is WLP the future of MEMS packaging? Or are hermiticity and materials challenges too much of an obstacle? This working group determined that the key topics for discussion were (in ranking order of importance): Cost and Performance Tradeoffs of Through-Silicon Vias (TSV); Capping Options; Where to do WLP; Temperature Challenges; and Microfluidics and Material Challenges.

More and more customers want smaller products with more functionality at a lower price. TSV is one way the MEMS industry is meeting this need. However, there are many challenges to TSV—yield, capping, production costs—and the group feels that it is not ready for primetime. For now it is best seen as niche technology, and its benefits are dependant upon device type.

According to the equipment manufacturers present in the group, the best solutions for capping are silicon and glass. While many universities are currently conducting research on polymer based capping methods, these methods have yet to be widely used in production.

While attendees could not decide on the best place to conduct WLP, they concurred that it is available at most wafer-level foundries. It was also agreed that high-volume devices drive its usage. One source of confusion was an issue of terminology—certain members use the phrase “Wafer-Level Packaging” while others use “Wafer-Level Capping.” It was recommended that MIG consult other industry sources to determine the appropriate nomenclature. Other recommendations include archiving white papers on the MIG website, and creating an application-specific best practices list.

TESTING A PACKAGE

When it comes to testing a traditional package there are several factors that affect reliability. This working group met to discuss testing challenges and deliver recommendations to MIG on how it might advance the industry. Several existing types of MEMS packaging were analyzed—traditional, WLP, open cavity, and polymer.

The primary challenges to traditional packaging are bonds, adhesives, and package-distorting sensing. Another problem occurs when customers use or test parts in unorthodox (i.e. previously untested) ways. WLP offers another set of obstacles, as a better understanding of the physics of failure are needed. It was suggested that guidelines on failure modes are needed to provide a roadmap on what to test. This would be beneficial since the industry needs to determine how to apply information from one product to another. It was mentioned that universities are working on materials research to understand what is happening at the micro level.

There were two key areas of disagreement. The most significant divergence revolved around the stages of testing—which aspect should be scrutinized first? The other disagreement had to do with an industry-wide study (of reliability and lifetime acceleration factors). Due to a reluctance to share proprietary information, such a study might not be feasible.

The group had many suggestions; most notably the implementation of an industry-wide, large-scale study of reliability factors in MEMS products. This would establish a resource of best practices and a database to help better understand the physics of failure. Others suggestions were to use a control plan to design for testability and built-in test, and to use process control to gate issues. Many members agreed that customer specifications do not have a centered test structure. It was suggested that statistical analysis be used to determine the parameter spread. The group recommended that further METRIC meetings with members representing all segments of the supply chain would be most beneficial.

PACKAGING STANDARDS

This working group met to discuss the pros and cons of packaging standards, particularly off-the-shelf and standard semiconductor packaging. The participants began by indentifying the different types of standards: documentary, test methods and terminology, standard reference materials, and products such as materials characterization. After a brief discussion, it was agreed that the industry places a higher priority on device design than on packaging.

The key challenge to standards has to do with cost—companies are reluctant to share their expertise as packaging is a competitive advantage. However, customers would like to see standards. Thus, standards may be more successful when applied to testing procedure instead of packaging styles. If the industry can find common ground on basic problems (i.e. non-proprietary), then standards may thrive in the MEMS industry (standards in the IC industry as evidence of this approach). Another challenge had to do with the industry: Is the MEMS industry's growth affected by a lack of standards? This question kept resurfacing during the discussion, and it was determined it is not (though standards could yield higher profits)...

As to be expected, there were a few disagreements. Packaging houses and customers disagreed on whether package designs should be standardized. The group could also not agree on who should be the driver—the manufacturers or the customers.

It was recommended that a coalition of forces within the MEMS industry be established. This coalition is necessary before any standards activities can be undertaken or enacted. It was also suggested that MIG conduct a survey on current standards; this information should be made available to all members. Finally, a tutorial on materials, fabrication, packaging, and testing would be useful.

STAY TUNED

MIG has already started working on some of the deliverables from METRIC 2008. With the creation of the MEMS Packaging Portal located in the members' only area of the MIG web site, we have already compiled a list of white papers and other resources on MEMS packaging. Stay tuned for a glossary of commonly used packaging terms and a members' capabilities database that will serve as a matchmaking tool among members as well as tool for promoting our members to potential industry partners.